Ctrl Alt Elite

System Design

11/16/18

Parts List:

Add: arithmetic unit used for addition operations

Sub: arithmetic unit used for subtraction operations

Left: arithmetic unit used for shift left operations

Right: arithmetic unit used for shift right operations

AND gate: used for logic AND function operations

OR gate: used for logic OR function operations

XOR gate: used for logic XOR function operations

NOT gate: used for logic NOT function operations

8:1 MUX: used to select the operation

A register: used for Num 1 input

B register: used for Num 2 input

select register: used for select bits

out register: used for final output

Input List:

A: holds input of first number

B: holds input of second number

select bits on MUX (S2, S1, S0): lists all operations to pick from

Rst: reset bit

Output List:

out: Result from operation or error, error is determined by most significant bit.

Interface List:

result register: Result of each operation carried into MUX.

Module List:

ALU module: Selects between different operations and assigns the results to output to be used in the testbenches.

testbench1 module: Displays labels, formats all output, tests all operations on two inputs (Num 1, Num 2) and shows an error for Add.

testbench2 module: Formats all output, tests all operations on two inputs (Num 1, Num 2) and shows an errors for both Add and Left Shift.

testbench3 module: Formats all output, tests all operations on two inputs (Num 1, Num 2) and shows no errors.

Mode List:

Ready: State before inputs go into operation state.

Add: State to perform addition on two inputs.

Sub: State to perform subtraction on two inputs.

Left: State to perform shift left on two inputs.

Right: State to perform shift right on two inputs.

AND: State to perform logical bitwise AND on two inputs.

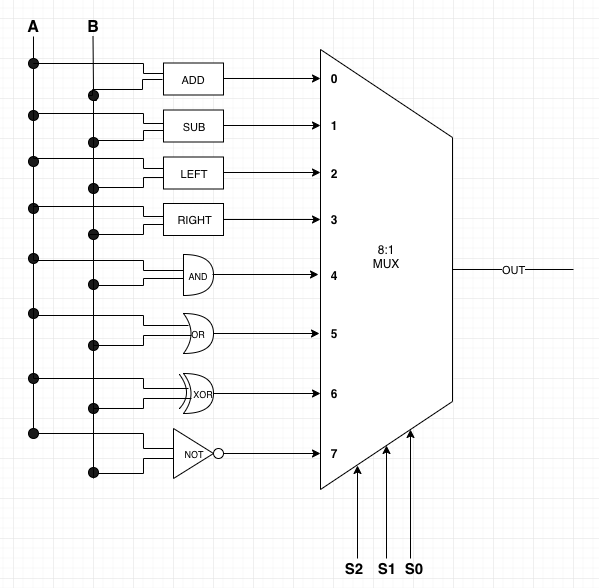
OR: State to perform logical bitwise OR on two inputs.

XOR: State to perform logical bitwise XOR on two inputs.

NOT: State to perform logical bitwise NOT on two inputs.

Error (overflow or carry): State to display error for Add and Left when output is 1XXXXXXXX.

Circuit Diagram:



State Machine:

